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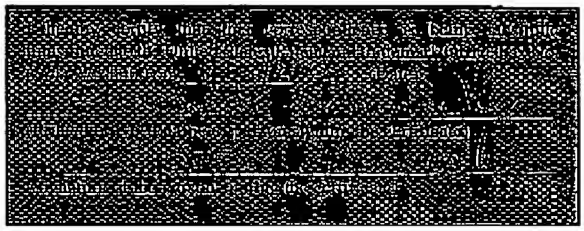
ATTORNEY DOCKET NO. TI 37479 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jiong-Ping Lu
Serial No.:	10/790,606
Filed:	March 1, 2004
Title:	SEMICONDUCTOR DEVICE HAVING A SILICIDED TGATE ELECTRODE AND METHOD OF MANUFACTURE THEREFOR
Grp./A.U.:	2818
Examiner:	Long K. Tran

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450



Sir:

AFFIDAVIT UNDER 37 C.F.R. §1.131

I, Jiong-Ping Lu, hereby state:

1. I am the inventor of the claimed subject matter in the Patent Application identified above and the inventor of the subject matter described therein.

2. Prior to September 24, 2003, I conceived of a method for manufacturing a semiconductor

device, the semiconductor device having a silicided gate electrode including at least a first metal and a second metal as covered by the above-identified Patent Application, as evidenced by the following:

I originally entered my idea on page 34 of my engineering notebook number LF920 on May 9, 2003, my idea being understood and witnesses by Dr. Haowen Bu. A true and correct copy of this page of my engineering notebook is attached hereto as Exhibit A. On or before May 24, 2003, I actually reduced to practice my idea. A true and correct copy of a task request, having an electronic file date of May 24, 2003, is attached hereto as Exhibit B. I manufactured product using my idea and sent it to Professor Kwong at UT Austin under a nondisclosure agreement on May 29, 2003. The manufactured product was received by UT Austin on May 30, 2003, as is evidenced by the true and correct copy of an email detailing receipt, which is attached hereto as Exhibit C. Soon thereafter, on or about November 21, 2003, I submitted an invention submission form disclosing my idea to the company that I work for. These notations are reflected in an invention submission form, which is kept in the regular course of business. A true and correct copy of an email illustrating the submission of the invention submission form is attached hereto as Exhibit D. Thereafter, I participated in preparing information necessary for subsequent filing of the above referenced Patent Application in the United States, which was diligently prepared and filed with the United States Patent Office on March 1, 2004.

3. I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by

fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the Application or any patent issuing thereon.

Jiong-Ping Lu

Date: 9-13-2005

LF920 34

ork of : [signature] Date: 5-9-2003

Alloying effect for metal gates

* We are collaborating with UT Austin on metal gates using full silicidation process. I am going to send some wafers to prof. Kwong at UT. He agreed that any IP come out of this project will belong to TI.

The following sample set may generate useful IP:

- Metal gates using Co/Ni stacks
- Metal gates using N_2-doped Ni

Both above stacks will then be silicided with doped poly to generate metal gates

The Co/Ni stack will have variable relative thickness

Haowen Bu 5-9-2003

Task 3726 Jiong-Ping
Lot 3055410

Wafer #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
HF dipping	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Co THK (A)	0	0	0	0	200	200	300	300	0	0	0	0	200	200	300	300	0	0	0	0	200	200	300	300
Ni THK (A)	600	600	300	300	100	100	0	0	600	600	300	300	100	100	0	0	600	600	300	300	100	100	0	0
TiN THK (A)	0	200	0	200	0	200	0	200	0	200	0	200	0	200	0	200	0	200	0	200	0	200	0	200

Process wafers in Lot 3055410 (PEMT2-8) using the following procedure

1. Check with MS to make sure MP17A will be available for steps 4 and 5, which will take about 45 minutes.
No engineering test will be needed after this process, as running wafers in this lot will not interfere production
2. Please plan your time so that step 5 will be run within one hour after completion of step 3
3. Send all wafers to HF dipping on **SH11D or SH18N: recipe 0315-060**
4. Run one burn-in (1K TEOS) with BS-NISTACK-C31 (or using automation: MP17A, burn-in-6352)
5. Trasnfer wafers to a green boat, process wafers in MP17A using the following sequences (no need for checking recipe time for this task):
   For wafers 1,9,17: ES-NI600
   For wafers 2,10,18: ES-NI600-TIN200
   For wafers 3,11,19: ES-NI300
   For wafers 4,12,20: ES-NI300-TIN200
   For wafers 5,13,21: ES-CO200-NI100
   For wafers 6,14,22: ES-200-100-200
   For wafers 7,15,23: ES-CO300
   For wafers 8,16,24: ES-CO300-TIN200
6. Store wafers in a PEMT rack

Lu, Jiong-Ping

From: Lu, Jiong-Ping
Sent: Friday, May 30, 2003 3:56 PM
To: 'huangchun wen'; 'Dim-Lee Kwong'
Cc: jang
Subject: New wafers

Huangchun and Johnny,

I forgot to mention in the earlier message about the process requirement for this new set of wafers. For wafers with 600A Ni (with/without TIN cap), please use similar process conditions you have been using, where NiSi is of primary interests. However, for all other wafers, di-silicide is the target phase, which requires higher process temperature and thinner metal films (that is why you see only 300A total metal thickness). You may experiment in the temperature range of 700C-950C for the di-silicide formation.

Please don't hesitate to contact me if you have any question.

Best regards,
Jiong-Ping

-----Original Message-----
From: huangchun wen [mailto:huangchun@mail.utexas.edu]
Sent: Friday, May 30, 2003 2:02 PM
To: Lu, Jiong-Ping; 'Dim-Lee Kwong'
Cc: jang
Subject: Re: Material analysis for UT ECE

Dear Dr.Lu,

Hi. Just to let you know that we got the wafers this morning.
Thank you very much.

Best regards,
Huangchun and Johnny

----- Original Message -----
From: Lu, Jiong-Ping
To: 'Dim-Lee Kwong'
Cc: jang ; 'huangchun wen'
Sent: Friday, May 30, 2003 10:38 AM
Subject: RE: Material analysis for UT ECE

Dear Prof. Kwong,

The new set of wafers was sent yesterday by FedEx (tracking #838546337989) and should arrive UT today. Attached is the split table. Please let me know if you have any question on the wafers.

Best regards,
Jiong-Ping

Lu, Jiong-Ping

From: Lu, Jiong-Ping
Sent: Friday, November 21, 2003 10:20 AM
To: Smith, Tina
Subject: Patent disclsoure submission: Dual work-function metal gates using Co-NI alloy fully silicidation

Tina,

Attached please find an electronic copy of a disclsoure, titled: " Dual work-function metal gates using Co-Ni alloy fully silicidation". I am sending you a hard copy with all signatures to your PC drop as well. Please let me know if you have any question.

Thanks and regards,
Jiong-Ping

Co-Ni-Si-alloy-F
JSI.doc (76 KB..